REMARKS

Support for the amendment of Claims 1, 13, 14, and 22 is found in the present application Specification at Page 56, lines 11 - 16. Support for the amendment of Claim 19 is found in the present application Specification at Page 55, lines 9 - 12, Page 56, lines 28 - 31, and Tables XV and XVI, for example. Support for new Claims 29, 30, 31, and 32 is found in the present application Specification at Page 56, lines 28 - 31, and in Tables XV and XVI, for example.

Applicants acknowledge that the earliest priority date for a particular subject matter contained in any of the applications under which the present application claims priority is the filing date of the application in which that subject matter first appeared.

Claim Rejections Under 35 USC § 102

Claims 1, 10, 11, and 13 - 16 are rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,143,476, to Ye et al.

Applicants respectfully contend that their invention as claimed in Claims 1, 10, 11, and 13 - 16 is not anticipated by Ye et al. The Ye et al. invention pertains to a method of patterning a semiconductor device feature where the patterned mask on the surface of a substrate to be etched is a high-temperature organic-based mask. This high-temperature, organic-based mask is used because it can be easily removed from the underlying substrate by exposure to an oxygen plasma. There are two paths by which the Ye et al. invention may be carried out. The first possibility is one in which the high-temperature organic-based mask is created by applying the high temperature organic-based masking material directly over the substrate to be etched; applying an inorganic hard mask material over the organic-based masking material; applying a photoresist over the inorganic hardmask material; using the photoresist to pattern the hardmasking material; removing the photoresist; and using the patterned inorganic hardmask to pattern the high-temperature organic-based masking material. The underlying substrate may be

etched without removal of the residual inorganic hardmask where the residual inorganic hardmask is completely removed, along with portions of the high-temperature, organic-based mask during the etching process. In the alternative, the inorganic hard mask may be removed prior to etching of the underlying substrate using the high-temperature, organic-based mask to pattern etch the underlying substrate. In the second path of the Ye et al. invention, the hard mask used to transfer a pattern to the underlying substrate is formed from a radiation sensitive high-temperature, organic-based masking material, which can be patterned by irradiation and development and used directly as the mask.

The present invention employs an inorganic masking layer directly on the surface of the substrate to be etched. There is no high-temperature, organic-based mask present on the surface of the substrate to be etched. All of applicants' presently pending independent claims specifically state that the mask layer consists essentially of an inorganic material. Thus, the Ye et al. disclosure teaches away from applicants' invention as described and claimed. Applicants' invention is not anticipated by the disclosure in the Ye et al. patent.

In more detail, the concept in the Ye et al. reference is that the hard masking layer is typically a good dielectric, and that the presence of the residual hard masking layer decreases the gate speed of a field effects transistor, for example. Thus, it is necessary to be certain that the residual hard masking layer can be easily removed. (Col. 2, lines 61 - 65) The Ye et al. method provides for a high-temperature, organic-based mask to be used for pattern transfer to an underlying substrate. In a first embodiment, a multi-layered masking structure is used which includes a layer of photoresist overlying a layer of inorganic masking material, where the inorganic masking material overlies a layer of high-temperature organic-based masking material which is patterned and used to transfer a pattern to an underlying substrate. This multi-layered masking structure is described at Col. 3, lines 48 - 60. In a second embodiment, the high-temperature pattern-imaging layer which is used to pattern a high-temperature organic-based masking material (which transfers the pattern to an underlying substrate) may also contain

organic components. This multi-layered masking structure is described at Col. 4, lines 47 -67, continuing at Col. 5, lines 1 - 8. When an inorganic hard masking material is used to pattern the high-temperature, organic-based mask, the inorganic hard masking material is designed to be removed prior to completion of etching of a substrate layer underlying the high-temperature, organic-based mask. Thus, it is always an organic-based mask layer residue which remains to be removed from the surface of an underlying substrate which has been pattern etched. (Col. 9, lines 41 - 47.) The Ye et al. reference teaches away from the present invention by teaching that it is a disadvantage to have an inorganic material applied directly over a conductive material during patterning of the conductive material, as the inorganic hard masking layer is difficult to remove subsequently. (Col. 2, lines 42 - 67)

In the "Response to Arguments" section, at page 8 of the present Office Action, the Examiner argues that applicants' claims are written in open language and are therefore inclusive or open-ended and do not exclude additional, unrecited elements of method steps. Applicants' independent Claims 1 and 14 have been amended to make it clearer that the mask layer and the protective layer recited in these claims consist essentially of inorganic materials. This eliminates the possibility of an inorganic mask layer overlying a high temperature, organic-based masking layer which is present on the surface of the protective layer, and eliminates the possibility that the protective layer could be a high-temperature, organic-based material. (Neither of these possibilities were described in applicants' Specification as originally filed and it was not intended that such embodiments be claimed.) In Claims 1 and 14, the substrate which is etched to form the RAM capacitor electrode is a noble metal layer underlying a protective layer.

Independent Claims 13 and 19 have been amended to recite "a substrate supporting a series of layers consisting essentially of a barrier layer on said substrate, a noble metal layer on said barrier layer, an inorganic mask layer on said noble metal layer, and a patterned resist layer on said mask layer".

It is applicants' contention that the amendments to independent Claims 1, 13, 14, and 19 made herein clarify that there is no organic-based mask in direct contact with the noble metal layer which is to be etched to form the RAM capacitor electrode.

The Ye et al. reference neither teaches or even suggests the specific combinations of materials and integrated processes which are taught by applicants. In light of the above distinctions and the amendments to independent Claims 1, 10, 13, and 14, applicants respectfully request withdrawal of the rejection of Claims 1, 10, 11, and 13 - 16 under 35 USC § 102(e), over Ye et al.

Claims 1, 10, 12 - 15, 17, and 22 are rejected under 35 USC § 102(b) as being anticipated by U.S. Patent No. 5,515,984, to Yokoyama et al.

Applicants respectfully contend that their invention as presently claimed in Claims 1, 10, 12 - 15, 17, and 22 is not anticipated by Yokoyama et al. The Yokoyama et al. reference discloses a method for etching a platinum film using a plasma generated from an etchant gas containing oxygen gas and chlorine gas or chloride gas, during which layers made of $PtCl_xO_y$ or a mixture containing $PtCl_x$ and PtO_y are formed on side walls of the etching resistant mask and the Pt film. The layers made of $PtCl_xO_y$ or a mixture containing $PtCl_x$ and PtO_y film, which are useful in profile control, are removed by a wet etch step after the etching of the platinum film. Applicants' invention as presently claimed does not include the use of oxygen as an etchant gas and therefore does not form the oxygen-containing compounds named in Yokoyama et al. As a result, applicants' method does not require the use of a wet etch step to remove these oxygen-containing materials from the sidewalls of the etched platinum structure. One of the best features of applicants' method is the reduction of residue formation during the etch process, which residues are difficult to remove after etch of the noble metal (platinum, for example but not by way of limitation).

In detail, the Yokoyama et al. reference discloses a method for etching a semiconductor structure where a platinum film has deposited thereover a thin film of a ferroelectric material such as PZT ($PbZr_xTi_{1-x}O_3$). An etch-resistant film such as spin on glass (SOG) is applied over the ferroelectric material; the etch-resistant film is patterned using a photoresist via known lithographic techniques. (Col. 3, line 41, through Col. 4, line 13) The ferroelectric film is plasma etched using the patterned etching resistant film as an etching mask, where the plasma source gas is a mixture of argon and chlorine gas. (Col. 4, lines 13 - 31) Specialized etch conditions are used so that the ferroelectric PZT layer will be properly etched. The platinum film is then plasma etched using a plasma source gas containing oxygen and a chlorine-containing gas at a substrate temperature in the range of 100°C to 400°C, during which layers of $PtCl_xO_y$ or $PtCl_x/PtO_y$ are formed on sidewalls of the etch-resistant film, the ferroelectric film, and the Pt film; and, the layers of $PtCl_xO_y$ or $PtCl_x/PtO_y$ are removed by performing a wet etch step. (Col. 5, lines 40 - 45)

In the "Background of the Invention", Yokoyama recites that etching of platinum in the past was done by wet etching with aqua regia (a mixture of nitric and hydrochloric acids, typically 1 part nitric acid to 3 or 5 parts hydrochloric acid), or ion milling with argon. These etch methods are said to cause a problem with a size shift in the pattern due to re-adhering of etched materials to the side walls of remaining portions of the Pt film after etching. (Col. 1, lines 26 - 33) Yokoyama et al. then recommends the use of dry etching to solve this problem; however, such dry etching is said to cause a tapering of the sidewalls of the etched platinum profile, which also causes a pattern shift. (Col. 1, lines 34 - 52)

Yokoyama et al. describes the plasma etch of platinum using a plasma source gas containing oxygen and chlorine or chloride gas, during which $PtCl_xO_y$ or $PtCl_x/PtO_y$ layers are formed on the sidewalls of the etching resistant film and the platinum film to achieve the desired etch profile. (Abstract) These layers must subsequently be removed by a wet etch. The wet etch is carried out using an aqueous solution of hydrochloric acid, sulfuric acid, phosphoric acid,

nitric acid, or the like. (Col. 5, lines 40 - 45) Yokoyama et al. is back to using a wet etch step similar to that which was which was said to cause problems in the beginning. Further, a wet etch requires that the substrate be removed from the plasma processing chamber and increases the expense of the device fabrication.

Applicants' invention as claimed in amended independent Claims 1, 13, 14, and 22 recites that the noble metal layer is plasma etched using a plasma generated from an etchant gas comprising a halogen gas; and a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof. Applicants' examples of the plasma etch step for etching a noble metal such as platinum teach the use of a plasma source gas of this composition at Page 56, lines 11 - 16; Page 57, lines 12 - 13; and Tables VI, XII, XIII, XIV, XV, XVI, and XVII, of applicants' Specification, for example and not by way of limitation.

Yokoyama et al. neither teaches nor even suggests the specific combination of etchant plasma source gases disclosed and claimed by applicants. All of the Yokoyama et al. etchant gases contain oxygen, which is not contained in applicants' etchant plasma source gases. The absence of oxygen, particularly in the etching of the noble metal platinum, in applicants' claims avoids the formation of etch byproducts which are particularly difficult to remove, requiring a wet etch, for example.

In light of the above distinctions and the amendments to independent Claims 1, 13, 14, and 22, applicants respectfully request withdrawal of the rejection of Claims 1, 10, 12 - 15, 17, and 22, under 35 USC § 102(b), over Yokoyama et al. on grounds of anticipation.

Claims 22, 23, and 25 - 28 are rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,004,882, to Kim et al.

Applicants respectfully contend that their invention as presently claimed in Claims 22, 23, and 25 - 28, is not anticipated by Kim et al. The Kim et al. reference discloses a method for etching a platinum film using a plasma generated from an etchant gas containing mixtures of

oxygen and chlorine (O_2/Cl_2), oxygen and hydrogen bromide (O_2/HBr), oxygen and bromine (O_2/Br_2), or oxygen and argon (O_2/Ar). Preferably, the etchant gas is O_2/Cl_2, where oxygen is 50 % or more of the total O_2Cl_2 mixture by flow rate. (Col. 2, lines 57 - 64, for example.) As discussed above, applicants do not use oxygen as their plasma source gas in the embodiments of the invention which are presently claimed.

In light of the above distinctions and the amendment to independent Claim 22, applicants respectfully request withdrawal of the rejection of Claims 22, 23, and 25 - 28 under 35 USC § 102(e) as being anticipated over Kim et al.

Claim Rejections Under 35 USC § 103

Claims 12 and 17 are rejected under 35 USC § 103(a) as being unpatentable over Ye et al.

The deficiencies of the disclosure of Ye et al. with respect to the patentability of the present invention are discussed in detail above with respect to the rejection of Claims 1, 10, 11, and 13 - 16 under 35 USC § 102(e), over Ye et al.

Claims 12 (which depends from Claim 1) and 17 (which depends from Claim 14), both pertain to the thickness of the inorganic mask layer which is applied over the inorganic protective layer which is applied over the conductive noble metal layer. Applicants respectfully contend that Claims 12 and 17 are patentable over Ye et al. for the same reasons that independent Claims 1 and 14 are patentable over Ye et al. (as discussed in detail above), regardless of the thickness of the inorganic masking layer. However, to meet the requirements with respect to an amendment after final rejection, applicants have cancelled these two claims, which are considered to be of lesser importance than other claims which applicants need to present at this time.

In light of the cancellation of Claims 12 and 14, the Examiner is respectfully requested withdrawal of the rejection of Claims 12 and 17 under 35 USC § 103(a), over Ye et al.

Claims 2 - 5 are rejected under 35 USC § 103(a) as being unpatentable over Ye et al., as applied to Claim 1, and further in view of U.S. Patent No. 6,046,113, to Hong et al.

Applicants respectfully contend that Claims 2 - 5 are not obvious over the combination of the Ye et al. and Hong et al. references. The Ye et al. reference teaches the requirement of a patterned high-temperature, organic-based masking layer directly overlying the substrate to be etched, while applicants apply their inorganic masking layer overlying the substrate to be etched. The Hong et al. reference teaches the use of a combination of anisotropic dry etching, followed by isotropic wet etching as a method of removing an outer layer from an inner surface during semiconductor fabrication. (Abstract and Col. 1, lines 45 - 50, for example). Applicants do not teach or claim the use of wet etchants. A combination of these two references, both of which teach away from applicants' invention, does not render applicants' invention as claimed in Claims 2 - 5 obvious.

In more detail, applicants' Claims 2 - 4 depend from Claim 1 and pertain to the use of an additional step in which residues from the noble metal layer etch step or residues from the protective layer etch step are removed prior to a subsequent etch step. Claim 5 depends from Claim 1 and recites that the protective layer is removed during pattern etching of the barrier layer. In any case, these claims are patentable over the Ye et al. reference for the reasons provided with respect to the patentability of Claim 1 over the Ye et al. reference. Further, a combination of the steps recited in the dependent claims with the steps recited in Claim 1 is distinctly patentable as an integrated process which is not described or even suggested in the Ye et al. reference.

The Hong et al. reference pertains to a method of etching layers during fabrication of a semiconductor device, which method employs a combination of dry and wet etch steps. (Col. 1, lines 45 - 50) Hong et al. is cited by the Examiner as teaching that residual layers remaining on a surface would interfere with later semiconductor processing. The need to remove residual layers during processing of a device structure has been generally recognized in the art. For example,

the Ye et al. reference teaches that the presence of a residual layer such as a photoresist is likely to interfere during subsequent pattern transfer steps which are conducted at temperatures which tend to melt or distort the photoresist. (Col. 4, lines 31 - 36)

However, the removal of layers which are not needed in the final device structure may occur during a series of integrated process steps only at a time such that the removal can be integrated into the process as a whole without harming the device structure which is to be obtained. Thus, it is the order in which a particular series of process steps is carried out which dictates when it is possible to remove undesired etch stack layers. The timing of the removal is unique to the structure being etched and to the manner in which etching is carried out. For example, applicants' etching is carried out using dry plasma etching, while the etching described in the Hong et al. reference is carried out using a combination of wet etching and dry etching. It is readily apparent to one skilled in the art, upon reading the disclosures of applicants and Hong et al., that the process steps required to get from applicants' starting structure to the final structure are totally different from those required in the Hong et al. reference.

The Examiner suggests that "It would have been obvious to one of ordinary skill in the art to remove the residual noble metal and residual protective layer in the method of Ye because Hong teaches that residual layers will interfere with later semiconductor processing". However, it is highly unlikely that one skilled in the art would combine the teachings in the Ye et al. reference with the teachings in the Hong et al. reference, due to the difference in device structure and etch methods described in these two references. Further, even if the teachings of these two references are combined, they do not lead in the direction of applicants' invention, since there is no organic mask material used in applicants' method and there is no wet etch process used in applicants' method.

In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claims 2 - 5 under 35 USC § 103(a), over Ye et al., and further in view of Hong et al.

Claim 19 is rejected under 35 USC § 103(a) as being unpatentable over Ye et al., in view of U.S. Patent No. 4,456,675, to Anderson, Jr. et al. and U.S. Patent No. 5,948,570, to Kornblit et al.

Applicants respectfully contend that Claim 19 of applicants' invention is not obvious in view of a combination of the Ye et al., Anderson, Jr. et al., and Kornblit et al. references.

Claim 19 is an independent claim which recites that an inorganic mask layer is deposited on the noble metal layer, and thus this claim is not obvious over the teachings of Ye et al. which requires that a high-temperature, organic-based mask layer is deposited on the substrate to be etched (such as a metal layer, for example). The Anderson, Jr. et al. process pertains to a "lift-off" process, where portions of a metal layer are removed by depolymerization of an underlying polymeric layer in the areas where the metal layer is to be removed. Applicants are using a dry etch process to pattern their noble metal and no lift-off process is even suggested. A combination of the Anderson, Jr. et al. and the Ye et al. references will not lead to applicants' invention.

The Kornblit et al. reference teaches a method of etching a chromium-comprising layer using reactive ion etching where the plasma is generated from a gaseous mixture of oxygen, chlorine, and nitrogen, where the patterned resist material is an organometallic material, such as a polymer which contains silicon or germanium. Applicants' plasma source gas as claimed in amended Claim 19 consists essentially of a halogen containing gas, a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof, and an additive gas selected from the group consisting of HBr, BCl_3, and mixtures thereof. Applicants' plasma source gas does not contain oxygen other than potential trace amounts which would not alter the etch process. Applicants' patterned mask is an inorganic mask, while the Kornblit et al. patterned mask is formed from an organic-containing material. The addition of the teachings of the Kornblit et al. reference with those of Ye et al. and Anderson, Jr. et al. does not motivate one skilled in the art to arrive at applicants' invention.

In more detail with respect to the Anderson Jr. et al. and Kornblit et al. references, the Anderson, Jr. et al. reference pertains to a process for forming a desired metal pattern on a substrate. The method comprises forming a mask of a thermally depolymerizable polymer on the substrate with a pattern of openings complementary to the desired metal pattern; blanket coating the substrate and the mask with a metal; heating the substrate to depolymerize the depolymerizable polymer; cooling the surface of the metal to delaminate the metal coated in areas where thermally depolymerizable polymer is present; removing the delaminated metal where necessary; and, optionally, plasma ashing the depolymerized polymer to remove residual depolymerized polymer from the substrate. (Abstract) This kind of process is often referred to as a "lift-off" process. There is no lift-off process involved in applicants' method. The lift-off process often leaves behind loose pieces of metal which are large enough to totally disrupt the function of a structure of the kind fabricated in the semiconductor industry today and is not in use for fabrication of the kinds of devices described by applicants.

Anderson, Jr. et al. is cited by the Examiner as teaching that silicon dioxide is a conventional etch stop material. Those skilled in the art would generally recognize that any material can be used as an etch stop material depending on the combination of gases which are used in the etch process. Whether silicon oxide could be an etch stop material is not an issue with respect to patentability of applicants' Claim 19.

Kornblit et al. is cited by the Examiner as teaching that a noble gas may be added to etchant gas mixtures in order to increase ion flux, stabilize the plasma, or both. Applicants would agree that it is generally known in the art that noble gases which are generally inert may be used as diluents within a plasma source gas. At the same time it is important to note that the Kornblit et al. plasma source gas contains oxygen which is not present in applicants' plasma source gas.

A combination of the Ye et al. method (which interposes an organic material layer between the hardmasking layer and underlying substrate to be etched) with the Anderson, Jr. et

al. process (which employs a metal lift off technique not used by applicants) and the Kornblit et al. process (which employs a different combination of etchant gases from those used by applicants) will not lead one skilled in the art to applicants' invention as claimed in Claim 19.

In the "Response to Arguments" section, at page 8 of the present Office Action, the Examiner states: "With respect to claim 19 and dependent claims, in response to the applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references." Applicants believe that they have demonstrated in detail above, with respect to the present rejection (and also with respect to other rejections which rely on a combination of references, in the present and previous Office Actions) that: a) one skilled in the art would not have a strong motivation to combine the references cited by the Examiner; and b) even if one skilled in the art were to combine the various cited references, the combined teachings of the references would not suggest applicants' claimed invention to one skilled in the art. This is particularly true where a portion of the references teach away from applicants' invention as presently claimed.

Applicants contend that as a part of determining what the combination of references teaches, one must first address what is taught in each reference. Only then is it possible to understand what is suggested or taught by the combination of the references. Further, unless there is some suggestion in the references themselves that the teachings in one reference should be combined with the teachings in another reference, then there is no grounds for making the combination. In the present instance, the combination of references cited does not even suggest to one skilled in the art which process variables or materials should be selected to arrive at applicants' invention. It is only with the hindsight of applicants' disclosure that the Examiner has gone to a variety of different references to look for particular elements of applicant's invention which might be combined with other elements found in separate disclosures to try to obtain a summation of parts which looks like applicants' invention. The Anderson, Jr. et al. lift off process has nothing to do with the etching of electrodes for a RAM capacitor. The Kornblit

et al. reference pertains to etching of noble metals such as chromium, but using an organic-based patterning mask (where applicants specifically use an inorganic-based patterning mask). One skilled in the art would be led away from applicants' invention by these references. If the Examiner is only using these references to illustrate particular variables which are adjusted within semiconductor processing schemes, then where is the suggestion in the art of the particular combination of variables which applicant uses to achieve the etching of noble metal electrodes in a RAM capacitor? How would one skilled in the art know which series of integrated process steps would provide the desired results, which etchants would provide reduced residue on the etched structure surface for the noble metals applicants used in their experimentation? If the answer to these questions does not spring forth from the references cited, then the Examiner has not met the requirements for establishing a prima facie case of obviousness. A basic mandate inherent in 35 U.S.C. §103 is that "a piecemeal reconstruction of prior art patents in the light of appellants' disclosure" shall not be the basis for a holding of obviousness. *In re Kamm and Young*, 452 F.2d 1052, 172 U.S. P.Q. 298, 301 (C.C.P.A. 1972). In the absence of evidence that suggests the desirability of combining references in a proposed manner, such combination is not available to preclude patentability under 35 U.S.C. §103. *King Instrument Corp. v. Otair Corp.*, 767 F.2d 853, 226 U.S.P.Q. 402 (Fed. Cir. 1985). To combine references (A) and (B) properly to reach the conclusion that the subject matter of a patent would have been obvious, case law requires that there must be some teaching, suggestion, or inference in either reference (A) or (B), or both, or knowledge generally available to one of ordinary skill in the relevant art that would lead one skilled in the art to combine the relevant teachings of references (A) and (B). A claim cannot properly be used as a blueprint for extracting individual teachings from references. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 227 U.S.P.Q. 657 (Fed. Cir. 1985). There must be some logical reason apparent from positive, concrete evidence of record that justifies a combination of primary and secondary references. *In re Laskowski*, 871 F.2d 115, 10 U.S.P.Q.2d 1397 (Fed. Cir. 1989).

The above combination of references is an example of an instance where individual teachings are taken from unrelated references to try to render obvious an applicant's invention. One skilled in the art of RAM capacitors is unlikely to combine these references, but even if the references are combined, it is well established in case law that "obvious to try" does not meet the requirement under 35 U.S.C. § 103 for obviousness. "The mere need for experimentation to determine parameters needed to make a device work is an application of the often rejected obvious-to-try standard and falls short of the statutory obviousness of 35 U.S.C. §103." (*Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).) "An 'obvious-to-try' situation exists when a general disclosure may pique the scientist's curiosity, such that further investigation might be done as a result of the disclosure, but the disclosure itself does not contain a sufficient teaching of how to obtain the desired result or indicate that the claimed result would be obtained if certain directions were pursued." (*In re Eli Lilly & Co.*, 902 F.2d 943, 14 U.S.P.Q. 2d 1741 (Fed.Cir. 1990).)

In light of the above distinctions and the amendment to Claim 19, applicants respectfully request withdrawal of the rejection of Claim 19 under 35 USC § 103(a), over Ye et al., in view of Anderson, Jr. et al. and Kornblit et al.

Claims 6, 9, and 18 are rejected under 35 USC § 103(a) as being unpatentable over Ye et al., as applied to Claim 1, and further in view of U.S. Patent No. 5,591,671, to Kim et al.

Applicants respectfully contend that Claims 6, 9, and 18 are not obvious over a combination of the Ye et al. and Kim et al. references. Claims 6, 9, and 18 all depend directly from Claim 1. Claim 6 recites that the mask layer is formed from CVD SiO_2; Claims 9 and 18 pertain to various materials which may be used to form the masking layer, where there are six different materials listed and only one of these is silicon oxide. Clearly claims 6, 9, and 18 are distinct from the Ye et al. reference, which teaches against the direct application of an inorganic masking layer over a substrate metal which is to be etched. The Kim et al. reference pertains to a

method of producing multi-layer metal connections using a dual damascene process. There is no description of the dry etching of electrodes of a RAM capacitor structure of the kind described by applicants. As a result, the method of fabricating the Kim et al. structure and the steps used in the method are considerably different from the steps described and claimed by applicants. A combination of the Kim et al. reference with the Ye et al. reference does not lead in the direction of applicants' invention.

The distinctions between the disclosure of Ye et al. and applicants' invention are discussed in detail above. Kim et al. pertains to a method for interconnecting layers in a semiconductor device which can form a low resistance contact. An insulating layer is formed on a semiconductor substrate, and an opening is formed in the insulating layer. The opening is a contact hole for exposing an impurity diffusion region formed on the semiconductor substrate, or a via hole for exposing a lower conductive layer formed on the semiconductor substrate. Subsequently, a titanium ohmic contacting layer and a titanium nitride barrier layer are formed on the semiconductor substrate. Thereafter, a refractory metal layer which completely fills the remainder of the opening hole is formed by depositing the refractory metal on the barrier layer. The resultant structure is heat-treated at a temperature above 450°C. As a result, oxidation of the ohmic contacting layer and the barrier layer is said to be prevented, and silicide is actively formed on the interface between the ohmic contacting layer and the silicon substrate. (Abstract)

Kim et al. is cited by the Examiner as teaching that CVD is a conventional method for depositing silicon oxide. The Examiner states "It would have been obvious to one of ordinary skill in the art in the method of Ye, Ye in view of Hong or Ye in view of Anderson and Kornblit to deposit the (second) mask layer of silicon dioxide using CVD because Kim teaches that this is a conventional deposition method for this material". As applicants described in their specification, and as claimed in Claims 9 and 18, CVD SiO_2 is only one of many masking materials which may be used. Other materials include TEOS, Si_3N_4, BSG, PSG, BPSG, and mixtures thereof. Applicants recited the use of CVD SiO_2 in Claim 6, because this method of

producing a mask integrates nicely with other deposition processes used to form the starting structure used by applicants, of the kind shown in Figures 1 and 2. The fact that a reference discloses the use of a material commonly used in semiconductor device fabrication does not render applicants' particular process obvious when the reference cited pertains to a different process and to fabrication of a different device than that described and claimed by applicants.

Applicants' claimed method is clearly distinguishable from the method described and claimed in the Ye et al. reference, and is clearly distinguishable from the method described and claimed in the Kim et al. reference. A combination of these references will not suggest to one skilled in the art to develop a completely different process of the kind described and claimed by applicants. If the Examiner could somehow put applicants' invention out of her mind for a few minutes and consider only the content of the Ye et al. and Kim et al. references combined, and then try to imagine a method of etching noble metal electrodes in a RAM capacitor, based on the disclosure in these references alone, it might become clearer that applicants' invention is not suggested by the combination of these two references.

In light of the above distinctions and the amendment to Claim 1, applicants respectfully request withdrawal of the rejection of Claims 6, 9, and 18 under 35 USC § 103(a), over Ye et al., and further in view of Kim et al.

Claims 7 and 8 are rejected under 35 USC § 103(a) as being unpatentable over Ye et al., in view of Hong et al., as applied to Claims 2 or 4, and further in view of Kim et al.

Applicants respectfully contend that Claims 7 which pertains to the ability to use the same oxide for the inorganic patterning mask overlying a noble metal to be etched as a RAM electrode and for the substrate layer which underlies a barrier layer over which the noble metal electrode material is deposited is not apparent from a combination of the disclosures in the Ye et al., Hong et al. and Kim et al. references. The description in Ye et al. recommends against using an inorganic patterning mask such as a silicon oxide mask over a metal surface to be etched in

general. The Hong et al. reference pertains to a method of removing an outer layer from an inner surface by anisotropically etching a portion of the outer layer and then etching a remaining portion of the outer layer using a wet etchant in a silicide formation process. (Col. 1, lines 15 - 17 and Col. 1, lines 52 - 57.) Applicants' method pertains to an 8 step integrated process for producing noble metal electrodes in a RAM capacitor structure. The limitations of applicants' Claim 1 and Claim 2 must be read into Claim 7 which depends from these claims. There is no wet etching step in the 8 process steps described and claimed by applicants, regardless of which materials make up various layers in the semiconductor structure of applicants. The materials which can be used in an integrated process depend on the integrated steps in the process. Materials which can be used in one series of process steps may fail miserably in a different process where the process step variables are different and the final resultant structure, which is required to exhibit a particular functionality, is different. There is no suggestion of applicants' final semiconductor structure or of applicants' integrated process for producing the structure in the Hong et al. reference. Combining the teachings of the Hong reference with the teachings of the Ye et al. reference does not provide a method of forming electrodes in a RAM capacitor using an inorganic patterning mask over the surface of a noble metal and then using solely dry etch processes for etching the noble metal into an electrode. As mentioned above, the Kim et al. reference discloses techniques for interconnecting layers in a semiconductor device. Once again, the integrated process for forming the structure and the materials which are used in the process, as well as the process variables as a whole are different.

Applicants' Claim 8 relates to the use of a silicon oxide inorganic hard mask for pattern etching the RAM electrode in a 9 step integrated process. The nine steps in the process are not taught or even suggested by a combination of the teachings in the three references cited.

The distinctions between the Ye et al. and Kim et al. references which were made above with respect to Claims 6, 9, and 18 further apply to Claims 7 and 8. In addition, the Hong et al.

reference, which pertains to a combination of wet and dry etch steps (while applicants' invention does not employ wet etch steps), has been distinguished above.

In light of the above distinctions and the amendment to Claim 1, applicants respectfully request withdrawal of the rejection of Claims 7 and 8 under 35 USC § 103(a), over Ye et al., in view of Hong et al., and further in view of Kim et al.

Claim 21 is rejected under 35 USC § 103(a) as being unpatentable over Ye et al., in view of Anderson, Jr. et al. and Kornblit et al., as applied to Claim 19, and further in view of Kim et al.

Applicants respectfully submit that Claim 21 is not obvious over this combination of references. Claim 21 recites the various materials which may be used to form the inorganic patterned mask layer recited in independent Claim 19. The distinctions between the invention claimed in Claim 19 and the disclosures of Ye et al., Anderson, Jr. et al., and Kornblit et al. were discussed in detail above with reference to Claim 19. As previously mentioned, the Kim et al. reference merely mentions that CVD is one of the techniques used to deposit silicon oxide, which is one of the six inorganic materials named in Claim 21. The fact that one of the materials which can be used to form the mask is mentioned with reference to a completely different semiconductor structure does not render applicants 6 step integrated process obvious. Since the teachings of Ye et al., Anderson, Jr. et al., and Kornblit et al. do not suggest the series of integrated process steps disclosed and claimed by applicants for forming noble metal electrodes in a RAM capacitor, adding the teachings of Kim et al. which pertain to a method of forming interconnects between layers of a semiconductor structure adds nothing to these teachings which would direct one skilled in the art to the integrated process claimed in Claim 19, or in Claim 21 which depends from Claim 19.

In light of the above distinctions and the amendment to Claim 19, applicants respectfully request withdrawal of the rejection of Claim 21 under 35 USC § 103(a) over Ye et al., in view of Anderson, Jr. et al. and Kornblit et al., and further in view of Kim et al.

Claim 20 is rejected under 35 USC § 103(a) as being unpatentable over Ye et al., in view of Anderson, Jr. et al., and Kornblit et al., as applied to Claim 19, and further in view of U.S. Patent No. 5,613,296, to Kurino et al.

Claim 20 recites the method of Claim 19, where the method additionally comprises a step of etching the etch stop layer underlying the barrier layer. As previously discussed in detail, the Ye et al., Anderson, Jr. et al., and Kornblit et al. reference combination does not render Claim 19 obvious. The addition of the Kurino et al. reference, which pertains to a dual damascene process for forming multilayered interconnects, does not render Claim 19, or Claim 20 which depends from Claim 19 obvious. While it may be useful to an Examiner to look for similar materials in other disclosures as a means of finding related art, when the related art does not disclose a similar end use device or structure to that of the claimed invention, and does not disclose a similar processing method to that of the claimed invention, it is unlikely that the related art would enable one skilled in the art to pull together the inventive method and device structure with the degree of success required to meet the requirements established by case law for an obviousness determination. As discussed above, obvious to try does not meet the requirements for obviousness under 35 U.S.C. § 103.

As discussed above, applicants' claimed method is clearly distinct from the method disclosed by Ye et al., and is not obvious over the method disclosed by Ye et al. Further, the addition of the disclosures of Anderson, Jr. et al. and Kornblit et al. do not lead toward applicants' invention. The Kurino et al. method pertains to another process which is totally unrelated to the formation of RAM capacitors of the kind described in applicants' invention. A combination of the teachings of these references as a whole is more confusing than helpful, since

the methods in the various references involve different process steps used in a different order than applicants' method, to produce a different result.

In light of the above distinctions and the amendment to Claim 19, applicants respectfully request withdrawal of the rejection of Claim 20 under 35 USC § 103(a), over Ye et al., in view of Anderson, Jr. et al. and Kornblit et al., and further in view of Kurino et al.

Applicants contend that the presently pending claims as amended are in condition for allowance, and the Examiner is respectfully requested to enter the requested amendments and to pass the application to allowance.

The Examiner is invited to contact applicants' attorney with any questions or suggestions, at the telephone number provided below.

Respectfully submitted,

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